

# [AI2 MAX: BFX-UA300]

## HDMI Physical Layer Compliance Test Guide

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Organization  
R&D Lab. 2

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Issued Date  
2021.01.11

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Version  
1.0

Revision History

| Version | Date       | Description                   | Owner      |
|---------|------------|-------------------------------|------------|
| 1.0     | 2021/01/11 | 1 <sup>st</sup> Draft version | Lonnie Kim |
|         |            |                               |            |
|         |            |                               |            |

# Physical Layer Compliance Testing



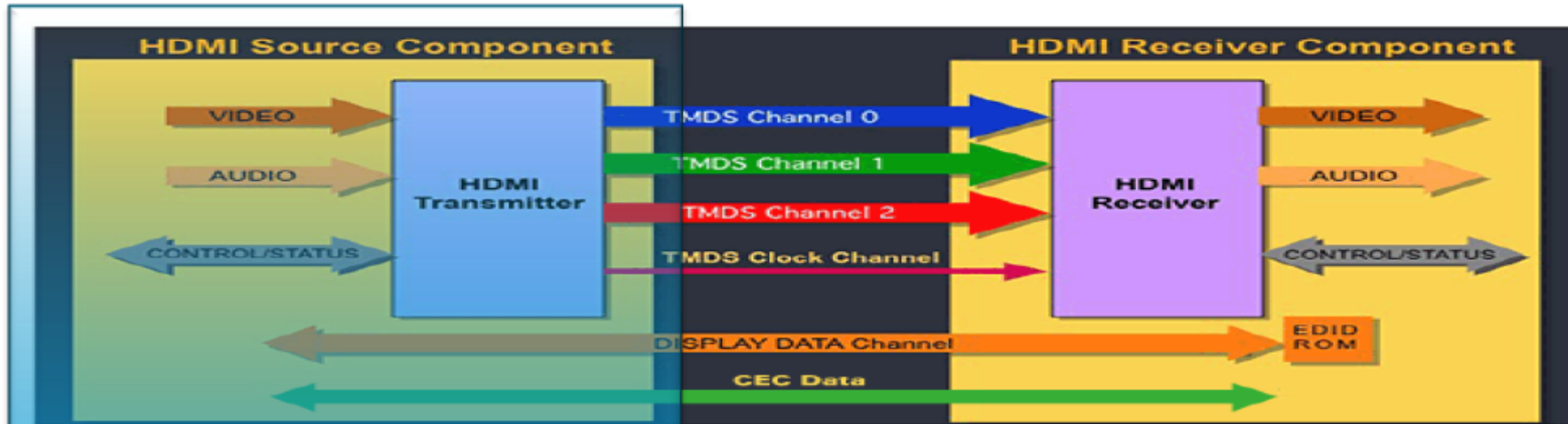
## Physical Layer Test Details

- **HDMI 2.0 includes a 3.4 Gbps to 6 Gbps data rate band specification.**
  - The new HDMI 2.0 Tx tests are called HF1-xx (Rx: HF2-xx)
  - The HDMI 1.4b Tx tests are TMDS 7-xx (Rx: 8-xx)



## Physical Layer Compliance Testing(1.4)

### ● Source Testing



### Source

- 7-4 : Rise/Fall Time
- 7-6 : Inter-pair Skew
- 7-8 : Clock Duty Cycle
- 7-9 : Clock Jitter
- 7-10 : Eye Diagram

**Differential**

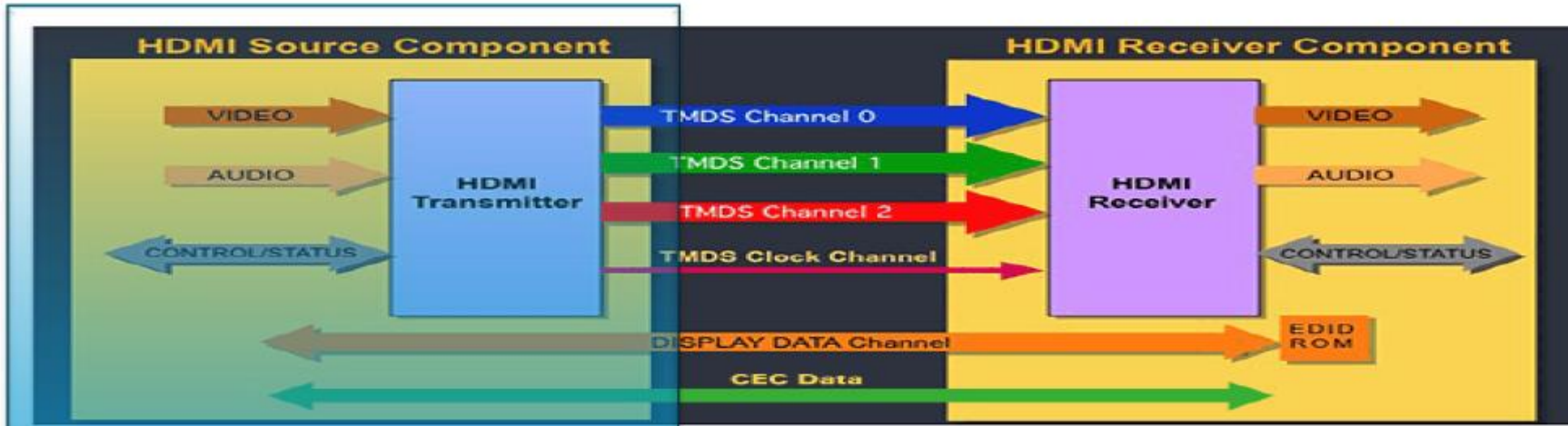
- 7-2 : Voltage VL
- 7-7 : Inter-pair Skew

**Single-ended**



## Physical Layer Compliance Testing(2.0)

### ● Source Testing



### Source

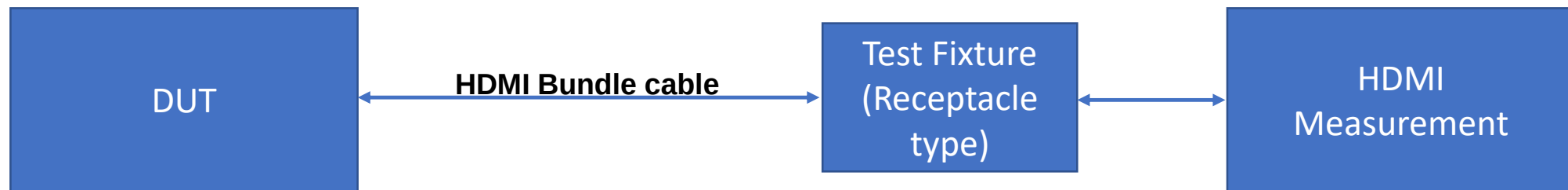
- **HF1-1 :  $V_L$  and  $V_{\text{Swing}}$**
- **HF1-2 :  $T_{\text{RISE}}$ ,  $T_{\text{FALL}}$**
- **HF1-3 : Inter-pair Skew**
- **HF1-4 : Intra-pair Skew**
- **HF1-5 : Differential Voltage**
- **HF1-6 : Clock Duty and Rate**
- **HF1-7 : Clock Jitter**
- **HF1-8 : Eye Diagram**

# **SK Broadband Compliance Testing Concept**



## Test Concept

- Resolution
  - 1080i/1080p/2160p
- Concept





## Testing Items(1.4)

### ● Source Testing

| Test Item | Test Name                          | Pass Limits                          | Actual Value | Margin |
|-----------|------------------------------------|--------------------------------------|--------------|--------|
| 1         | 7-9: Clock Jitter                  | VALUE <= 0.25Tbit                    |              |        |
| 2         | 7-4: Clock Rise Time               | VALUE >= 75.000 ps                   |              |        |
| 3         | 7-4: Clock Fall Time               | VALUE >= 75.000 ps                   |              |        |
| 4         | 7-8: Clock Duty Cycle(Minimum)     | >=40%                                |              |        |
| 5         | 7-8: Clock Duty Cycle(Maximum)     | <=60%                                |              |        |
| 6         | 7-10: D0 Mask Test                 | No Mask Failures                     |              |        |
| 7         | 7-10: D0 Data Jitter               | <=0.3Tbit                            |              |        |
| 8         | 7-4: D0 Rise Time                  | VALUE >= 75.000 ps                   |              |        |
| 9         | 7-4: D0 Fall Time                  | VALUE >= 75.000 ps                   |              |        |
| 10        | 7-10: D1 Mask Test                 | No Mask Failures                     |              |        |
| 11        | 7-10: D1 Data Jitter               | <=0.3Tbit                            |              |        |
| 12        | 7-4: D1 Rise Time                  | VALUE >= 75.000 ps                   |              |        |
| 13        | 7-4: D1 Fall Time                  | VALUE >= 75.000 ps                   |              |        |
| 14        | 7-10: D2 Mask Test                 | No Mask Failures                     |              |        |
| 15        | 7-10: D2 Data Jitter               | <=0.3Tbit                            |              |        |
| 16        | 7-4: D2 Rise Time                  | VALUE >= 75.000 ps                   |              |        |
| 17        | 7-4: D2 Fall Time                  | VALUE >= 75.000 ps                   |              |        |
| 18        | 7-2: VL Clock +                    | LowerLimit V <= VALUE <= 2.900 V     |              |        |
| 19        | 7-2: VL Clock -                    | LowerLimit V <= VALUE <= 2.900 V     |              |        |
| 20        | 7-7: Intra-Pair Skew - Clock       | -150 mTbit <= VALUE <= 150 mTbit     |              |        |
| 21        | 7-2: VL D0+                        | LowerLimit V <= VALUE <= 2.900 V     |              |        |
| 22        | 7-2: VL D0-                        | LowerLimit V <= VALUE <= 2.900 V     |              |        |
| 23        | 7-7: Intra-Pair Skew - Data Lane 0 | -150 mTbit <= VALUE <= 150 mTbit     |              |        |
| 24        | 7-2: VL D1+                        | LowerLimit V <= VALUE <= 2.900 V     |              |        |
| 25        | 7-2: VL D1-                        | LowerLimit V <= VALUE <= 2.900 V     |              |        |
| 26        | 7-7: Intra-Pair Skew - Data Lane 1 | -150 mTbit <= VALUE <= 150 mTbit     |              |        |
| 27        | 7-2: VL D2+                        | LowerLimit V <= VALUE <= 2.900 V     |              |        |
| 28        | 7-2: VL D2-                        | LowerLimit V <= VALUE <= 2.900 V     |              |        |
| 29        | 7-7: Intra-Pair Skew - Data Lane 2 | -150 mTbit <= VALUE <= 150 mTbit     |              |        |
| 30        | 7-6: Inter-Pair Skew - D0/D1       | -200 mTpixel <= VALUE <= 200 mTpixel |              |        |
| 31        | 7-6: Inter-Pair Skew - D1/D2       | -200 mTpixel <= VALUE <= 200 mTpixel |              |        |
| 32        | 7-6: Inter-Pair Skew - D0/D2       | -200 mTpixel <= VALUE <= 200 mTpixel |              |        |



## Testing Items(2.0)

### ● Source Testing

| Test Item | Lane Name | Test Name                      | Pass Limits                | Actual Value | Margin |
|-----------|-----------|--------------------------------|----------------------------|--------------|--------|
| 1         |           | HF1-1- VL and Vswing           |                            |              |        |
|           | Clock     | TMDS VLow for Clock+           | 2.300V~3.100V              |              |        |
|           |           | TMDS VLow for Clock-           | 2.300V~3.100V              |              |        |
|           |           | Vswing for Clock+              | 200.000mV~600.000mV        |              |        |
|           |           | Vswing for Clock-              | 200.000mV~600.000mV        |              |        |
|           | D0        | TMDS VLow for D0+              | 2.300V~2.900V              |              |        |
|           |           | TMDS VLow for D0-              | 2.300V~2.900V              |              |        |
|           |           | Vswing for D0+                 | 400.000mV~600.000mV        |              |        |
|           |           | Vswing for D0-                 | 400.000mV~600.000mV        |              |        |
|           | D1        | TMDS VLow for D1+              | 2.300V~2.900V              |              |        |
|           |           | TMDS VLow for D1-              | 2.300V~2.900V              |              |        |
|           |           | Vswing for D1+                 | 400.000mV~600.000mV        |              |        |
|           |           | Vswing for D1-                 | 400.000mV~600.000mV        |              |        |
|           | D2        | TMDS VLow for D2+              | 2.300V~2.900V              |              |        |
|           |           | TMDS VLow for D2-              | 2.300V~2.900V              |              |        |
| 2         |           | Vswing for D2+                 | 400.000mV~600.000mV        |              |        |
|           |           | Vswing for D2-                 | 400.000mV~600.000mV        |              |        |
|           |           | HF1-2- TRISE, TFALL            |                            |              |        |
|           | Clock     | Clock Rise Time                | VALUE >= 75.000 ps         |              |        |
|           |           | Clock Fall Time                | VALUE >= 75.000 ps         |              |        |
|           | D0        | D0 Rise Time                   | VALUE >= 42.500 ps         |              |        |
|           |           | D0 Fall Time                   | VALUE >= 42.500 ps         |              |        |
|           | D1        | D1 Rise Time                   | VALUE >= 42.500 ps         |              |        |
|           |           | D1 Fall Time                   | VALUE >= 42.500 ps         |              |        |
|           | D2        | D2 Rise Time                   | VALUE >= 42.500 ps         |              |        |
|           |           | D2 Fall Time                   | VALUE >= 42.500 ps         |              |        |
| 3         |           | HF1-3- Inter-Pair Skew         |                            |              |        |
|           | D0        | Inter-Pair Skew: D0-D1         | VALUE <= 0.2000 Tcharacter |              |        |
|           | D1        | Inter-Pair Skew: D1-D2         | VALUE <= 0.2000 Tcharacter |              |        |
|           | D2        | Inter-Pair Skew: D0-D2         | VALUE <= 0.2000 Tcharacter |              |        |
| 4         |           | HF1-4- Intra-Pair Skew         |                            |              |        |
|           | Clock     | TMDS Intra-Pair Skew for Clock | VALUE <= 25.2528ps         |              |        |
|           |           | TMDS Intra-Pair Skew for Clock | VALUE <= 0.15TBit          |              |        |
|           | D0        | TMDS Intra-Pair Skew for D0    | VALUE <= 25.2528ps         |              |        |
|           |           | TMDS Intra-Pair Skew for D0    | VALUE <= 0.15TBit          |              |        |
|           | D1        | TMDS Intra-Pair Skew for D1    | VALUE <= 25.2528ps         |              |        |
|           |           | TMDS Intra-Pair Skew for D1    | VALUE <= 0.15TBit          |              |        |
|           | D2        | TMDS Intra-Pair Skew for D2    | VALUE <= 25.2528ps         |              |        |
|           |           | TMDS Intra-Pair Skew for D2    | VALUE <= 0.15TBit          |              |        |

| Test Item | Lane Name | Test Name                                       | Pass Limits          | Actual Value | Margin |
|-----------|-----------|-------------------------------------------------|----------------------|--------------|--------|
| 5         |           | HF1-5- Differential Voltage                     |                      |              |        |
|           | Clock     | Clock Minimum Differential Voltage              | VALUE >= -780.0000mV |              |        |
|           |           | Clock Maximum Differential Voltage              | VALUE <= 780.0000mV  |              |        |
|           | D0        | D0 Minimum Differential Voltage                 | VALUE >= -780.0000mV |              |        |
|           |           | D0 Maximum Differential Voltage                 | VALUE <= 780.0000mV  |              |        |
|           |           | D0 Data Jitter                                  | N.A.                 |              |        |
|           |           | D0 Data Jitter                                  | N.A.                 |              |        |
|           | D1        | D1 Minimum Differential Voltage                 | VALUE >= -780.0000mV |              |        |
|           |           | D1 Maximum Differential Voltage                 | VALUE <= 780.0000mV  |              |        |
|           |           | D1 Data Jitter                                  | N.A.                 |              |        |
|           |           | D1 Data Jitter                                  | N.A.                 |              |        |
|           | D2        | D2 Minimum Differential Voltage                 | VALUE >= -780.0000mV |              |        |
|           |           | D2 Maximum Differential Voltage                 | VALUE <= 780.0000mV  |              |        |
|           |           | D2 Data Jitter                                  | N.A.                 |              |        |
|           |           | D2 Data Jitter                                  | N.A.                 |              |        |
| 6         |           | HF1-6- Clock Duty Cycle and Clock Rate          |                      |              |        |
|           | Clock     | Maximum Duty Cycle                              | VALUE <= 60.00%      |              |        |
|           |           | Minimum Duty Cycle                              | VALUE >= 40.00%      |              |        |
| 7         |           | Clock Rate                                      | 85MHz~150Mhz         |              |        |
|           |           | HF1-7- Clock Jitter                             |                      |              |        |
|           | Clock     | TMDS Clock Jitter at TP2                        | VALUE <= 50.5056ps   |              |        |
|           |           | TMDS Clock Jitter at TP2                        | VALUE <= 0.30000TBit |              |        |
| 8         |           | TMDS VSwing at TP1                              | 400.00mV ~ 1200.00mV |              |        |
|           |           | HF1-8- Data Eye Diagram                         |                      |              |        |
|           | D0        | TMDS Data Eye Diagram Delay on Positive D0 Lane | VALUE <= 0 Hits      |              |        |
|           |           | TMDS Data Eye Diagram Delay on Negative D0 Lane | VALUE <= 0 Hits      |              |        |
|           | D1        | TMDS Data Eye Diagram Delay on Positive D1 Lane | VALUE <= 0 Hits      |              |        |
|           |           | TMDS Data Eye Diagram Delay on Negative D1 Lane | VALUE <= 0 Hits      |              |        |
|           | D2        | TMDS Data Eye Diagram Delay on Positive D2 Lane | VALUE <= 0 Hits      |              |        |
|           |           | TMDS Data Eye Diagram Delay on Negative D2 Lane | VALUE <= 0 Hits      |              |        |

**Thank you.**